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(Rebecca Bechtelar)

#### COMPILATION TECHNIQUES FOR RECONFIGURABLE ARCHITECTURES (HARDBACK)



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Springer-Verlag New York Inc., United States, 2008. Hardback. Condition: New. 2009 ed.. Language: English. Brand New Book. The extreme? exibility of recon?gurable architectures and their performance pot- tial have made them a vehicle of choice in a wide range of computing domains, from rapid circuit prototyping to high-performance computing. The increasing availability of transistors on a die has allowed the emergence of recon?gurable architectures with a large number of computing resources and interconnection topologies. To - ploit the potential of these recon? gurable architectures, programmers are forced to map their applications, typically written in high-level imperative programming I- guages, such as C or MATLAB, to hardware-oriented languages such as VHDL or Verilog. In this process, they must assume the role of hardware designers and software programmers and navigate a maze of program transformations, mapping, and synthesis steps to produce ef?cient recon?gurable computing implementations. The richness and sophistication of any of these application mapping steps make the mapping of computations to these architectures an increasingly daunting process. It is thus widely believed that automatic compilation from high-level programming languages is the key to the success of recon?gurable computing. This book describes a wide range of code transformations and mapping te- niques for programs described in high-level programming languages, most - tably imperative languages, to recon?gurable architectures.



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