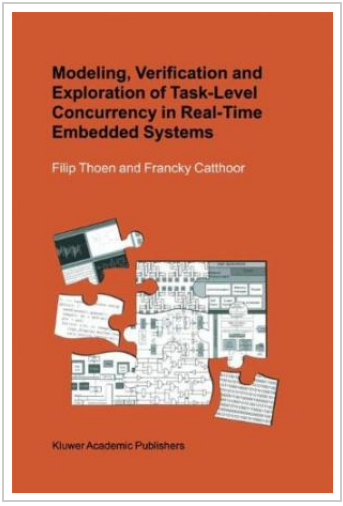

Modeling, Verification and Exploration of Task-Level Concurrency in Real-Time Embedded Systems

By Francky Catthoor

Springer. Hardcover. Condition: New. 438 pages. Dimensions: 9.2in. x 6.1in. x 1.0in.The combination of VLSI process technology and real-time digital signal processing (DSP) has brought a break-through in information technology. This rapid technical (r)evolution allows the integration of ever more complex systems on a single chip. However, these technology and integration advances have not been matched by an increase in design productivity, causing technology to leapfrog the design of integrated circuits (ICs). The success of these emerging systems-on-a-chip (SOC) can only be guaranteed by a systematic and formal design methodology, possibly automated in computer-aided design (CAD) tools, and effective re-use of existing intellectual property (IP). In this book, a contribution is made to the modeling, timing verification and analysis, and the automatic synthesis of integrated real-time DSP systems. Existing literature in these three domains is extensively reviewed, making this book the first to give a comprehensive overview of existing techniques. The emphasis throughout the book is on the support and guaranteeing of the real-time aspect and constraints of these systems, which avoids time consuming design iterations and safeguards the ever shrinking time-to-market. The proposed Multi-Thread Graph (MTG) system model features two-layers, unifying a (timed) Petri net and a control-data flow...

Reviews

Good eBook and helpful one. It really is writter in straightforward words and phrases and never confusing. I am just effortlessly could possibly get a enjoyment of looking at a published book.

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