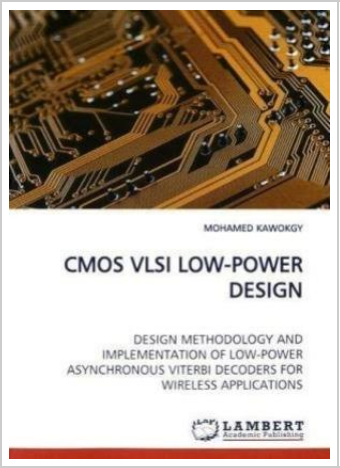

CMOS VLSI LOW-POWER DESIGN

By ELKAWOKGY, MOHAMED

Condition: New. Publisher/Verlag: LAP Lambert Academic Publishing | DESIGN METHODOLOGY AND IMPLEMENTATION OF LOW-POWER ASYNCHRONOUS VITERBI DECODERS FOR WIRELESS APPLICATIONS | Power dissipation is a critical parameter in digital design for the implementation of high performance portable, battery operated systems, such as wireless communications systems. Clocked or synchronous digital designs consume a significant amount of power associated with coordinating the operation of millions of transistors at GHz clock rates. Besides, the operating speed of such systems is limited by the slowest functional logic unit. By contrast, asynchronous designs are active only when doing useful work, enabling considerable savings in power and operating at the average speed of all components. Yet, the overhead associated with the asynchronous control units implementing the handshaking protocol, in terms of silicon area, speed and power, as well as the lack of Computer Aided Design (CAD) tools for use in such designs have limited the use of asynchronous techniques. In this book, the author describes the concept and challenges of asynchronous VLSI CMOS circuit design and presents a complete design methodology to overcome such challenges via the design and implementation of a 64-state, 1/2-rate Viterbi decoder suitable for wireless communications applications. | Format: Paperback | Language/Sprache:...

Reviews

Extensive information for book fans. It is writter in basic words and never hard to understand. It is extremely difficult to leave it before concluding, once you begin to read the book.

-- ***Otis Wisoky***

This publication is great. It is full of wisdom and knowledge You will not really feel monotony at at any time of the time (that's what catalogs are for relating to when you ask me).

-- ***Dr. Everett Dicki DDS***