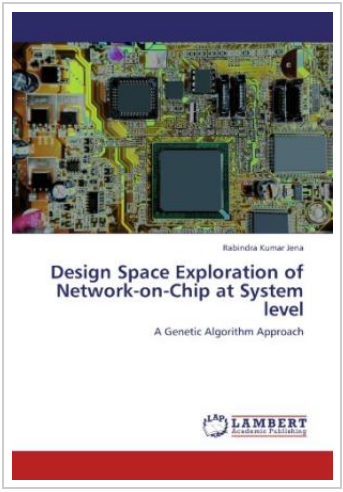

Design Space Exploration of Network-on-Chip at System level

By Rabindra Kumar Jena

LAP Lambert Academic Publishing Jan 2012, 2012. Taschenbuch. Book Condition: Neu. 220x150x10 mm. Neuware - About the Book: The goal of this text is to help students, researchers and academicians, who are working in the field of CAD for VLSI. Network-on-Chip(NoC) has been recently developed as an on-chip communication solution for System-on-Chip(SoC) design. This paradigm supports various communication resources at a time and overcomes the limitations of bus-based System. Design space exploration methodology at system level reduces the time-to-market pressure of the large and complex systems. On the other hand, design space exploration at system level is a combinatorial optimization problem. So, multi-objective Genetic Algorithm has been considered as an optimization tool for the design space exploration task. This book provides detailed methodology/algorithms to explore the design space of NoC at System Level using Genetic Algorithm. This book is the outcome of my PhD work. I hope this book will help all stake holders for extensive research in the field of NoC at System level. 160 pp. Englisch.

Reviews

This book is great. It is writter in simple words and not difficult to understand. I discovered this pdf from my dad and i suggested this ebook to find out.
-- ***Prof. Webster Barrows***

This ebook is fantastic. We have read and i also am confident that i am going to going to read through again yet again in the future. I am easily can get a pleasure of reading a published ebook.
-- ***Heloise Dare***